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Precision, Damage-Free Etching by Electron-Enhanced Reactions: Results and Simulations

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Ion-enhanced dry etch methods inflict "etch process damage" through surface ion bombardment. These inherent limitations in conventional dry etch methods create potential roadblocks to achieving device properties necessary for scaling below 32 nm. We describe an alternative dry etch method in which electrons with energies below about 100 eV stimulate precision etching of features as small as 20 nm without damage. This Low Energy Electron Enhanced Etching (LE4) method also gives atomically smooth etched surfaces, very high selectivity between materials, and maintains stoichiometry of compound materials. LE4 etches low K dielectric materials with no loss of carbon, and gives Line Width Roughness (LWR) values dramatically smaller than achieved by ion-enhanced etching. We have developed the Electron Force Field (eFF) method to describe electron dynamics in highly excited electronic states, and use it to show preferential bond breaking and product desorption after electronic excitation of the sample surface.

Introduction and Differentiation of LE4 Technology

Since the founding of the IC industry, etching technology has evolved in response to demands for controlling the critical dimensions (CD) and etched profiles of device features. Initially wet etching was used to define features some tens to hundreds of micrometers in size, and the loss of exact dimensions at the edges of these large features due to undercut by isotropic etching was acceptable. For sub-micrometer features anisotropic etching was necessary to control dimensions and profiles, and for these purposes ion-enhanced plasma etching was developed in the forms of Reactive ion etching (RIE) and inductively coupled (ICP) plasma etching. Ion enhanced etching gave excellent anisotropic profiles but inflicted damage on the wafer due to momentum transfer from bombardment by the energetic ions in the plasma. Now that device features in production have reached below 35 nm and are aiming toward 22 nm and below, there is need to further reduce and if possible completely eliminate etch damage and produce extremely smooth etched surfaces.

In confronting these etch demands, all versions of ion-enhanced plasma etching face certain challenges. Ion impact generates heat, so wafers must be cooled on the backside.

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Line edge roughness (LER), bowing, and notching limit the accuracy of CD control. Surface damage, lattice damage, and changes in stoichiometric composition of compound materials all trace to ion bombardment. Ion-induced alteration of material composition is a concern in etching low k dielectrics for interconnects applications as well as high k dielectrics in advanced gate stack configurations (1). Chloro-fluorocarbon etch residues require post-etch cleaning, and generate hazardous wastes harmful to the environment. The tools have become quite complex, requiring three or more RF generators to control the ion energy.

As an alternative to ion-enhanced etching, LE4 has the potential to avoid or meet these challenges, and the commercial tools for LE4 are expected to be less complex. The conceptual basis of LE4 is sketched in Figure 1. LE4 proceeds by a fundamentally different mechanism than the sub-surface collision cascades initiated by momentum transfer from ion bombardment (2). Instead of ion bombardment, etch products are removed by electron-enhanced desorption. If ion-enhanced etching can be considered a chemically reactive analog of sputtering, then LE4 can be considered a chemically reactive analog of Electron Stimulated Desorption (ESD), which has been extensively studied in surface science (3). These desorption processes are stimulated by electronic excitation of quantum transitions at the wafer surface, and they are controlled by material-specific energy thresholds. These thresholds provide the opportunity to tailor the electron energy to particular materials and thereby achieve high specificity and selectivity between different materials.

Initial tests of these concepts of LE4 were carried out in an ultrahigh vacuum system equipped with an electron gun, a molecular beam source to deliver etchant species, a differentially pumped quadrupole mass spectrometer to detect etch products, and several *in situ* components for surface analysis (4). A beam of hydrogen and a beam of low energy electrons were directed to an atomically clean Si(100) surface at room temperature. Figure 2 shows the results of each beam alone and the two beams together. Neither beam alone leads to etch products but together the two beams cause various SiH_x species to depart the surface, as a consequence of electron-enhanced etching.

Insight into the LE4 process is provided by *in situ* surface analysis. Examination of the initial surface by Low Energy Electron Diffraction (LEED) showed a pattern with the 4-fold symmetry of the Si(100) surface and the features of the Si(100)-(2×1) surface reconstruction due to Si-Si dimers formed between dangling bonds on the atomically clean surface. Examination by LEED after an extended period of etching as in Figure 2 showed the Si(100)-(1×1) pattern, in which the dimer bonds have been broken and the surface has only the 4-fold symmetry of the Si(100) surface. This means that the surface layer after etching has the same two-dimensional unit cell as the Si(100) layers in the bulk. The Si(100)-(1×1) LEED pattern is well known for Si(100) surfaces on which adsorbed H atoms have stabilized the dangling bonds and prevented dimer formation. Ultraviolet photoelectron spectroscopy (UPS) performed *in situ* confirmed the presence of Si-H bonds on the post-etch surface. The sample was rotated to face the mass spectrometer and subjected to a heating program to perform *in situ* temperature programmed desorption spectroscopy (TPD). Molecular hydrogen and fragments of SiH_4 were detected leaving the surface. After the TPD measurement, the sample was examined once again by LEED, and showed the Si(100)-(2×1) pattern characteristic of the atomically clean surface.

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This sequence of tests showed that LE4 removed material from the sample, and produced a H-terminated Si(100) etched surface. A simple annealing process desorbed the hydrogen and restored the (2×1) structure of the pristine surface before etching commenced. This result is significant because it demonstrates that LE4 has not disrupted the structure of the single crystal while etching away material. This is in dramatic contrast to ion bombardment of semiconductor surfaces; for example Ar^+ ion bombardment of Ge(111) surfaces at energies as low as 20 eV severely degraded the LEED patterns (5).

Practical applications of LE4 require a plasma configuration to overcome the limitations of the low flux and small spot size of the electron and molecular beams. We have developed a prototype LE4 plasma source in which the wafer is placed on a sample support in the positive column region of a normal DC glow discharge. See Figure 3. Operating pressure is in the range 10 – 100 mTorr. Plasma density on the order of 10^{+17} m^{-3} is achieved by using patented permeable hollow cathodes to generate large emission current at low voltage, typically 200 V – 1000 V (6). This plasma source is remote in the sense that the wafer is distant from the plasma electrodes. Electrical bias applied to the sample stage as a non-sinusoidal pulsed waveform draws electrons from the plasma to stimulate LE4 and draws positive ions as needed for charge neutralization. The energy of the electrons is adjusted to match surface excitation energies to enable LE4, and the energy of the ions is kept low to prevent ion-enhanced etching or damage during charge neutralization. Backside cooling is not necessary because there is no wafer heating due to momentum transfer from ion bombardment. The sample stage can be heated from 25 C to 250 C, to assist surface diffusion of etchant species and reactive intermediates. The next section illustrates applications of LE4 achieved with this prototype source.

We note that in 1979 Coburn and Winters demonstrated electron-enhanced etching of Si, SiO_2, and Si_3N_4 using an electron beam in a background of XeF_2, along with their demonstration of ion-enhanced etching with a beam of Ar^+ ions and a beam of XeF_2 (7). Their interest at that time was to test possible modes of radiation-enhanced etching in plasma reactors, and they did not examine the mechanism of electron-enhanced etching. Subsequent evolution in dry etching methods has revealed the need to eliminate damage in ion-enhanced etching and justifies the development of LE4 as a damage-free practical alternative.

Illustrative Applications of LE4 Technology

Profile Control and Line Width Roughness (LWR) in Si

In work reported previously, LE4 has achieved high-resolution feature definition in silicon using Cl_2/Ar gas mixtures and electron energy bias slightly higher than the empirically determined threshold (8). Anisotropic etching in LE4 depends on acceleration of electrons from the plasma to the wafer and does not require sidewall passivation. Figure 4a shows a cross section of 150 nm lines etched in Si with an amorphous carbon mask. The etched sidewalls are vertical and smooth, and there is no discernible faceting or disruption of the mask. Figure 4b shows cross sections of 50 nm lines etched with the same mask and the same process as in Figure 4a. The sidewalls are vertical and smooth, but there is a foot at the bottom of each line. Work is in progress to quantify aspect-ratio

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dependent etching (ARDE) to determine whether LE4 can reliably etch adjacent features of different sizes to the same depth and with vertical sidewalls to the bottom. Surveying a broad range of process conditions has revealed no cases of trenching, notching, or bowing in LE4.

Line width roughness (LWR) is a challenge in fine-line definition. Photoresists for 193 nm deep UV exposure are damaged in the earliest stages of ion-enhanced etching to cause LWR, which hinders the control of critical dimensions (9). Instead of re-working the entire lithographic process, a cost-effective solution would be to find an etch process that can correct the effects of LWR. To evaluate this approach with LE4, an oxide hard mask was applied over poly Si, and the hard mask was patterned by ion-enhanced etching from a photoresist mask. Figure 5a shows a top view of a 60 nm line, which has LWR = 10 ± 1 nm. These samples were subjected to LE4 using $H_2/Cl_2/Ar$ gas mixtures with the sample temperature at 45 C and the electron energy bias above the threshold for etching silicon but below the threshold for etching oxide. Figure 5b shows that LWR in the hard mask was substantially reduced to 2.1 ± 0.3 nm while the exposed poly Si was etched. This amounts to 80% reduction in LWR with LE4 relative to ion-enhanced etching. The LE4 results for 60 nm lines area already close to meeting the LWR = 1.8 specifications for the 22 nm node. Because the LE4 process just described is not sufficiently energetic to etch oxide films, we speculate that atoms at the sharp asperities at the edges of the hard mask are less stable than more fully bonded atoms in the film "bulk" and therefore have lower thresholds for LE4. Consequently atoms in the asperities should be etched more easily and first. This proposed mechanism for smoothening during LE4 is being investigated.

Ultrasmall Structures in Si

LE4 has defined structures as small as 20 nm in Si(100) using a mask generated from naturally occurring protein material (10). Certain classes of bacteria have an outer surface layer (the S-layer) that comprises a monolayer of protein with a highly ordered array of nanopores. Remarkably, these bacteria have generated pore patterns with each of the standard two-dimensional symmetries familiar in solid state physics, and within each symmetry a range of pore sizes and lattice constants (11). By selecting specific bacteria, one can obtain S-layers with specific pore symmetry and pattern dimensions. Wafers of Si(100) were cleaned and stripped of native oxide, then intentionally oxidized to create a thinner hydrophilic oxide layer that was coated with an S-layer having HCP symmetry with pore diameter 5 nm and lattice constant 20 nm. The S-layer was flashed with 1.2 nm of Ti metal, which was allowed to oxidize to total mask thickness of 3.5 nm. The masked wafers were subjected to LE4 using a H_2/He gas mixture. AFM imaging displayed the hexagonal pattern of pores before and after LE4, but the small pore diameter prevented AFM analysis of etch depth. The samples were cross-sectioned, thinned, and analyzed by high-resolution transmission electron microscopy (HR-TEM). The image in Figure 6 shows that the pattern from the S-layer was etched to a depth of 10 nm, but vertical sidewalls were not obtained. The diagonal lines in the figure are the lattice fringe lines from the Si crystal, which reach the perimeters of the etched holes. These lines at the perimeters of the etched holes demonstrate that the lattice structure of the crystal adjacent to the etched holes has not been disrupted by LE4. This is a clear demonstration of damage-free etching. In comparison, images of identically prepared samples subjected to ion-enhanced etching showed that the mask was partly destroyed, no lattice fringes

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existed near the etched holes, and a layer of sub-surface amorphous material has been generated. These are clear demonstrations of structural damage inflicted by ion-enhanced etching, but not by LE4.

Atomically Smooth Etching of SiO_2

In addition to control of critical dimensions, LE4 gives atomically smooth etched surfaces. Silicon dioxide deposited on Si(100) by PECVD was patterned with photoresist to define open areas approximately 3 mm × 3 mm. These samples were etched to a depth of 200 nm by LE4 using $H_2/Cl_2/Ar$ gas mixtures with the sample temperature at 45 C and the electron bias energy slightly higher than the empirically determined threshold for silicon dioxide. Imaging the bottom of the etched feature by AFM showed the surface to be atomically smooth with RMS surface roughness ~ 1.5Å. See Figure 7.

Previous work has shown that LE4 with chlorine-based recipes etches GaAs (100) and GaN(0001) to atomic smoothness (12, 13).

Damage-free Etching of Low K Dielectric Films

The damascene process for copper interconnects requires that dielectric films be etched with trenches of specified dimensions; copper is deposited into these trenches to form the interconnect lines. To prevent crosstalk between lines, the carbon is added to the dielectric films to reduce the dielectric constant below the value for SiO_2. Ion-enhanced etching removes the carbon through ion bombardment, as well as causing additional structural damage, and degrades the carefully tailored value of the dielectric constant. FTIR spectroscopy detects loss of carbon, as well as structural changes in the Si-O bond network. (14) Various low K dielectric films have been examined by FTIR before and after etching by LE4. Figure 8 shows the results for a SiCOH material etched to depths of 33 nm and 50 nm. No etch damage is discernible in the FTIR spectra.. No SiCOH peaks were removed. No new peaks appeared. There is no significant peak due to adsorbed water after atmospheric exposure. The LE4 processes are stable and reproducible. In addition to maintaining the low K material properties, LE4 has the potential to etch low K dielectrics with minimum LWR to minimize electron scattering at rough edges that reduces the conductivity of the damascene copper.

Key Results in Work Reported Previously

Simple *p*-*n* diodes of GaN grown on sapphire prepared for deposition of metal contacts by etching the *p*-GaN layer by LE4 had a turn-on voltage of 6 V compared to 12 V for the samples prepared by ion-enhanced etching. Damage-free etching reduced the contact resistance of these diodes, and enabled operation at lower power. or by ion-enhanced etching. (8)

LE4 chemistry is governed by material specific energy thresholds, which enables ultra-high selectivity etching, as illustrated by 150 nm thick poly Silicon over SiO_2, with a hard mask on the poly Si. SEM images show the poly Si is removed completely and there is no measurable loss of oxide and no discernible damage to the oxide, even at 100% overetch. Ion-enhanced etching does not achieve comparable selectivity between poly Si and oxide. (8)

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LE4 and ion-enhanced etching have comparable efficiency, so properly designed and optimized tools from the two approaches will produce comparable etch rates. This is reassuring in view of the very different fundamental microscopic mechanisms that drive ion-enhanced etching and LE4. (8)

Summary of Applications

The specific results described in the preceding section illustrate the achievements of LE4, as well as its potential performance advantages compared to ion-enhanced etching. We summarize these results in broader terms, and mention additional results not shown above, as follows:

- Excellent anisotropy and profile control in etching Si, SiO_2, and III-V materials without sidewall passivation
- Atomically smooth etched Si and SiO_2 surfaces (RMS: 1.3 - 3.2 Å)
- Atomically smooth etched GaAs and GaN surfaces (RMS: 2.5 - 4.0 Å)
- 20-nm silicon structures etched to atomic smoothness without damage
- Superior electrical properties after damage-free etching
- High selectivity of silicon to oxide by adjusting electron energy to specific thresholds
- Selectivity of semiconductors and insulators to organic and inorganic mask materials
- Etch efficiencies comparable to ion-enhanced tools
- Maintain surface stoichiometry in etching GaAs and GaN

These results show that LE4 has the potential for performance advantages in practical applications. Scientifically, a number of fundamental mechanistic questions remain to be studied. These are quite interesting since they involve chemical reactions occurring in excited quantum states at the surface. Special interest attaches to understanding the mechanism by which semiconductors and dielectrics are etched to atomic smoothness.

Mechanism of LE4

The LE4 process was designed to achieve damage-free etching by eliminating ion bombardment, and the inherent momentum transfer that causes damage, by introducing a different mechanism to achieve anisotropic etching and profile control in device features. In LE4, etching occurs when low energy electrons enhance the reaction of the wafer surface with chemically reactive etchants by stimulating excited electronic states. Momentum transfer from the electrons to the surface is negligible.

LE4 can be regarded as a chemically reactive analog of Electron Stimulated Desorption (ESD) of adsorbates from surfaces. The simplest model of ESD, the Menzel-Gomer-Redhead (MGR) mechanism (3), envisions a chemisorption bond holding an adsorbed atom to the surface, and assumes that electron bombardment stimulates one-electron transitions from the ground state to an excited state of that bond. If the potential energy in

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the excited state is repulsive (as in an anti-bonding molecular orbital), the chemisorption bond breaks, and the adsorbate departs from the surface.

The MGR mechanism provides a qualitative picture to guide simple interpretations of LE4 in terms of potential energy curves. But calculating or simulating the stationary states and associated potential energy curves for realistic etching systems, and describing dynamics in terms or transitions and curve crossings between these states, require a more sophisticated approach.

For such applications, the electron force field (eFF) method has been developed (15,16). The eFF method is an approximation to quantum mechanics specifically designed for simulations of excited state in complex materials within a classical molecular dynamics scheme. Each electron is represented by a Gaussian wave function, while nuclei are represented as point charges. Effective potential fields include electrostatic contributions, a special term to describe Pauli repulsion between electrons (the Gaussian wave functions are not antisymmetrized), and kinetic energy terms that arise from the quantum uncertainty principle. Dynamics are described by semiclassical wave packet motions. The method is highly efficient, and can describe system with thousands of electronic and nuclei.

The Auger excitation process involves some of the same key issues as LE4, and provides a test case to illustrate the eFF method (17). A primary incident electron ionizes a core state, a valence electron falls down to fill the core hole, and a second valence electron (the Auger electron) is ejected with kinetic energy uniquely determined by the energy states of the atom. The atom is left in an excited state with two holes. The ejected electrons are the basis of Auger Electron Spectroscopy used to identify the composition of surfaces. Ordinary quantum mechanics can calculate the energy spectra but cannot describe dissociation dynamics in the two-hole state.

We have used the eFF method to examine the Auger excitation process and its consequences in a diamondoid nanocluster model $C_{197}H_{112}$ that is fully saturated on the surface with H atoms and roughly spherical (18). It contains six distinct layers, ranging in depth from the center of the particle to the surface (Figure 9). By ionizing core electrons in each of these layers, we study surface vs. bulk effects, including the range over which surface bonds can be broken as a result of a core ionization.

Figure 10 shows how the eFF method tracks motions of the electrons in the Auger process after C1s core ionization. The valence electron represented in red fills the core within 3 fs after ionization, and the Auger electron represented in green is ejected within 7 fs. The remaining valence electrons represented in blue and purple stay in bonds to the same nucleus, but remain highly excited more than 50 fs after the core ionization. These excited electrons lead to bond breaking and fragmentation.

We used coupled electron and nuclear motions to track fragmentation of the cluster. Figure 11 shows the atomic composition of fragments released at time > 50 fs after core ionization of C atoms located at each of 6 depth positions. Excitation at an outer layer produces hydrogen and carbon fragments with yields of 0.67C, 0.17CH, and 0.02 CH_2 per core ionization. The charge state of the H products is also shown. The results are as follows. H and H^+ come from surface excitation. $H^-$and slow electrons are the only

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species that come from bulk excitation. The fact that the polyatomic fragment CH_2 comes only from surface excitation suggests a possible explanation for the atomic smoothness of surfaces etched by LE4, as described above.

Studies on carbon model clusters have shown that eFF captures the essence of the LE4 process.
(1) electron enhanced etching occurs through fragmentation and desorption processes in highly excited electronic states; (2) excitations at different sites induce fragments with different compositions to be desorbed from the surface; (3) Polyatomic fragments depart from surface atoms. eFF investigations of electron-induced decomposition of Si slabs with various surface terminations and adsorbates are under way

Outlook for LE4 Technology

Three general features of LE4, coupled with the applications demonstrated above, suggest that LE4 has the potential to become a production-level etch process. First, the equipment is considerably simpler and less expensive to manufacture and maintain than ion-enhanced etching tools, and should scale reliably to 300 mm wafers. Plasma generation in the source requires only DC power supplies. Long experience with sputtering equipment demonstrates that DC plasma scales up to larger dimensions with uniform performance more easily than high-frequency ac plasmas. The wafer bias method used in LE4 does not require a matching network. Backside cooling of the wafer is not necessary. Second, because the electrons are accelerated to the wafer by positive bias pulses, LE4 should avoid the electron-shading phenomenon and the resulting effects on etch profile and gate oxide breakdown that occur in ion-enhanced etching with sinusoidal applied bias and the resulting negative off-set bias (19). The absence of trenching, notching, and bowing effects bear out this possibility, and it is important to carry out future tests on oxide breakdown to determine the extent to which LE4 has indeed solved this class of problems. Third, the results achieved to date have relied upon simple etch chemistry recipes that do not leave residues on the wafer or on the plasma chamber walls. This eliminates the need for post-etch cleaning and simplifies overall process flow. In addition, the LE4 process can be used as a damage-free cleaning method to remove photoresist and residues from other process steps.

As a production-level tool, LE4 is a potential solution to the following applications, which challenge ion-enhanced etching:

- Increase selectivity to ultra-thin mask materials as features shrink
- Increase etch uniformity for 300 mm tools
- Eliminate charging damage and gate dielectric breakdown
- Limit sidewall and interfacial roughness on etched surfaces
- Remove masks and residues during process sequence without damage

LE4 provides high-resolution feature definition without damage, excellent selectivity between materials, and smooth etched surfaces all of which are necessary to meet the current and projected etch demands.

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References

1. Several important articles are in *Materials, Technology, and Reliability of Low-k Dielectrics and Copper Interconnects*, T.Y. Tsui, Y.-C. Joo, L. Michaelson, M. Lane, and A.A. Volinsky, Editors, Materials Research Society Symposium Proceedings, **914**, Warrendale, PA (2006).
2. C. Steinbrüchel, *Appl. Phys. Lett*,. **55**, 1960 (1989).
3. R.D. Ramsier and J.T. Yates, Jr., *Surf. Sci. Rep.*, **12**, 243 (1991).
4. H.P. Gillis, J.L. Clemons, and J.P. Chamberlain, *Jour. Vac. Sci. Technol. B*, **10**, 2729 (1992).
5. R.L. Jacobson and G.K. Wehner, *J. Appl. Phys*,. **36**, 2674 (1965).
6. H.P. Gillis, D.A. Choutov, and K.P. Martin, US Patent No. 5917285.
7. J.W. Coburn and H.F. Winters, *J. Appl. Phys.*, **50**, 3189 (1979).
8. H.P. Gillis, Samir J. Anz, and Matthew Demine, ECS Transactions **13(8),** 35 (2008).
9. M.-C. Kim, D. Shamiryan, J. Jung, W. Boullart, C.-J. Kang, and H.-K. Cho, *J. Vac. Sci. Technol. B*, **24**, 2645 (2006).
10. T.A. Winningham, H.P. Gillis, D.A. Choutov, K.P. Martin, J.T. Moore, and K. Douglas, *Surf. Sci.*, **406**, 221 (1998).
11. U.B. Sleytr *et al*., *FEMS Microbiology Rev.*, **20**, 151 (1997).
12. H.P. Gillis, D.A. Choutov, K.P. Martin, and Li Song, *Appl. Phys. Lett.*, **68**, 2255 (1996).
13. H.P. Gillis, D.A. Choutov, K.P. Martin, M.D. Bremser, and R.F. Davis, *J. Electronic Mater.*, **26**, 301 (1997).
14. J. Bao et al, Jour. Vac. Sci.Techno. **B26**, 219 (2008).
15. J.T. Su and W.A. Goddard III, Phys. Rev. Lett. **99,** 185003 (2007)
16. J.T. Su and W.A.Goddard III, J.Chem. Phys. **131,** 244501 (2009).
17. H.J. Mathieu, *Auger Electron Spectroscopy*, Ch.2 in J.C. Vickerman and I.S. Gilmore (eds) Surface Analysis (2^{nd} ed), Wiley, 2009.
18. J.Su and W.A. Goddard III, Proc. Natl. Acad. Sci. USA **106,** 1001 (2009)
19. K.P. Giapis, in *Handbook of Advanced Plasma Processing Techniques,* R.J. Shul and S.J. Pearton, Editors, p. 257, Springer-Verlag, New York (2000).

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Figures

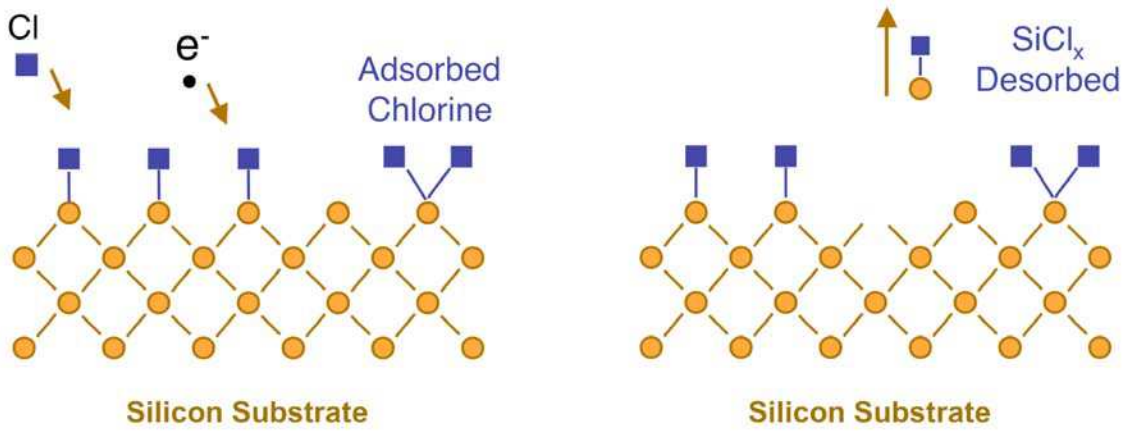

Figure 1. Conceptual representation of the LE4 process. The wafer is sketched in side view. Etchant species such as Cl atoms have adsorbed to the surface to form etch products, which are then removed by ESD.

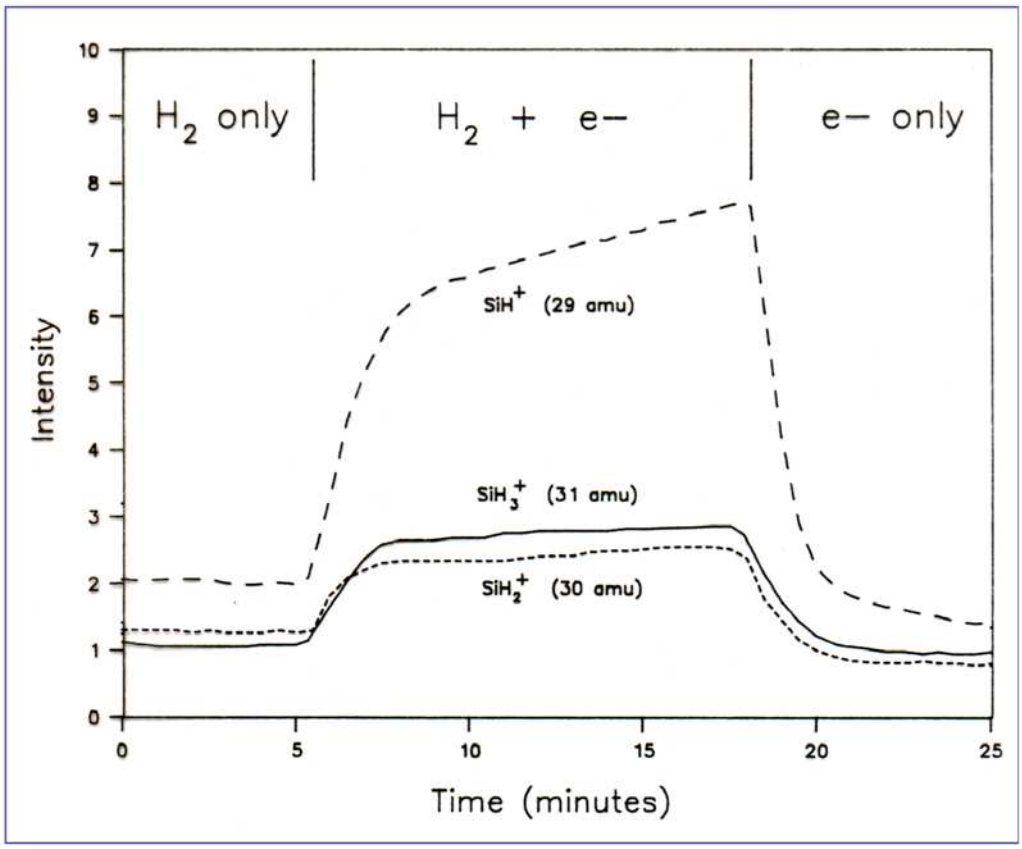

Figure 2. Electron-enhanced etching of Si(100) with hydrogen. Adapted from Reference 5.

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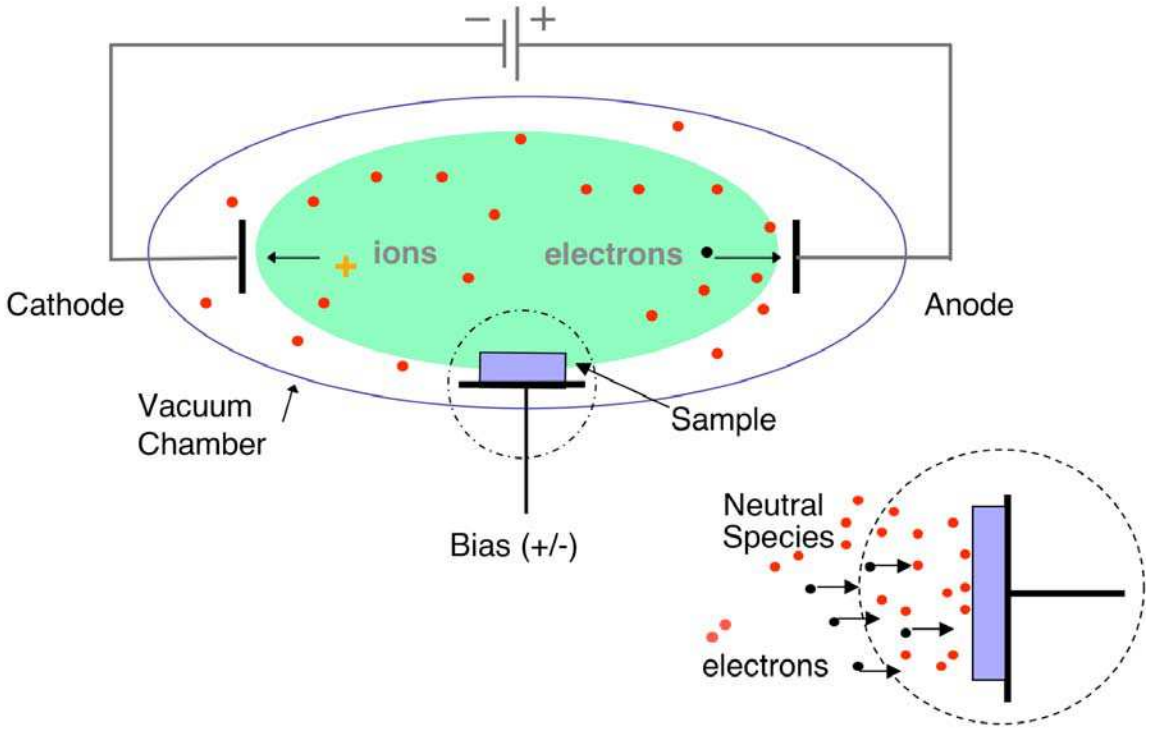

Figure 3. Schematic of the prototype LE4 plasma etch tool. Neutral reactants such as Cl atoms diffuse to the sample while electrons are accelerated by the applied bias.

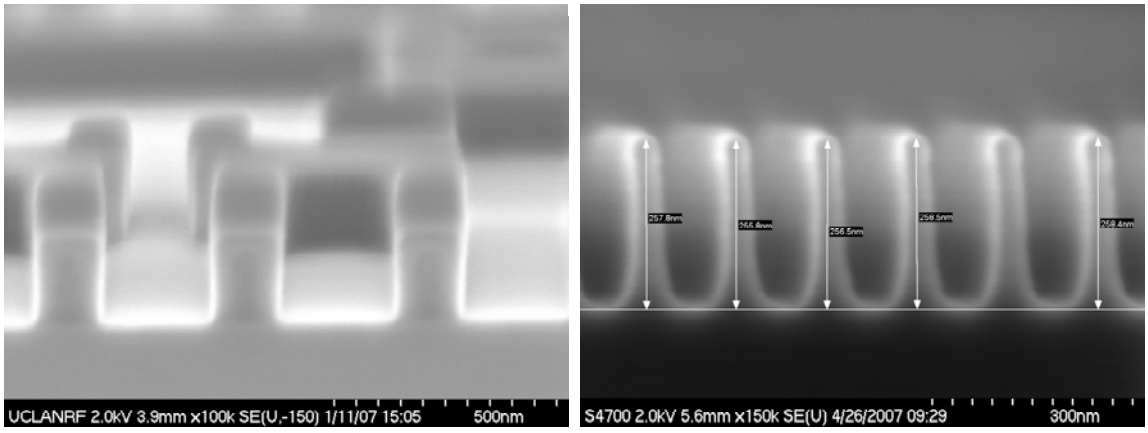

Figure 4. Silicon profile control by LE4. (a) Lines 150 nm wide etched in Silicon by LE4 . (b) Lines 50 nm wide etched in Silicon by LE4.

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